Advanced-Packaging Memory Solutions Targeting High Performance Applications

ConFab 2015

SK hynix

Agenda

- **Announcement**
- **Developments in Packaging Technology – Memory ICs**
- **Challenges Addressed by TSV**
- **Memory Solutions Utilizing TSV Technology**

Mass Production of the World 1st HBM

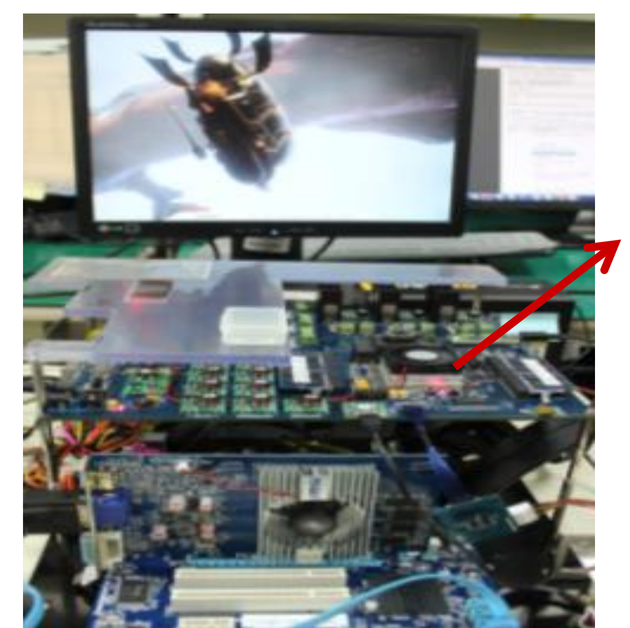
SK hynix completed the qualification for mass production in March 2015

SK hynix World-First HBM Products

- Worldwide first HBM provider
- Mass Production start from Apr 2015
- HBM2 design wins in progress with major SoCs in multiple market segments

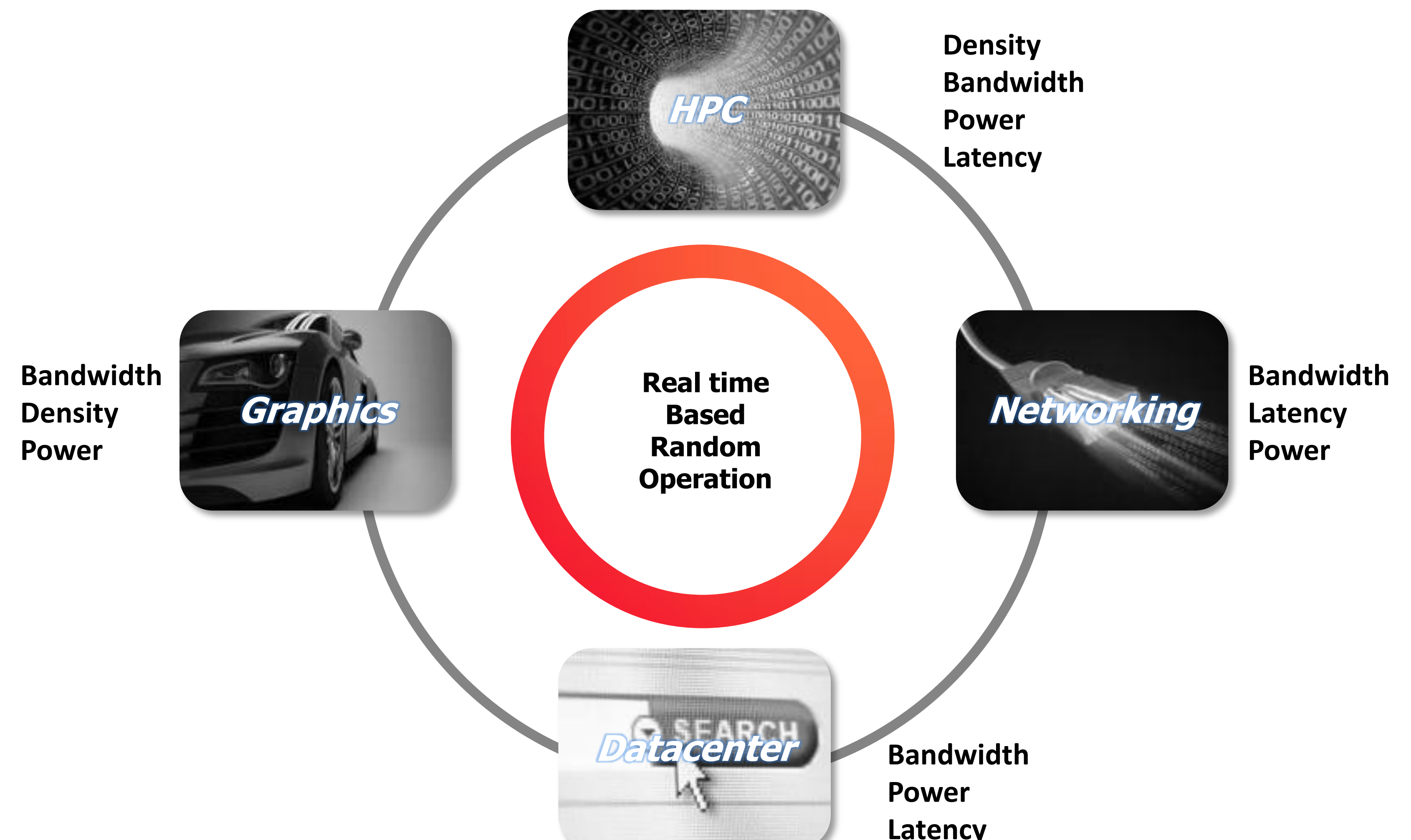
System Level Test Environment

- SK hynix in-house test board for HBM



General Memory Requirements

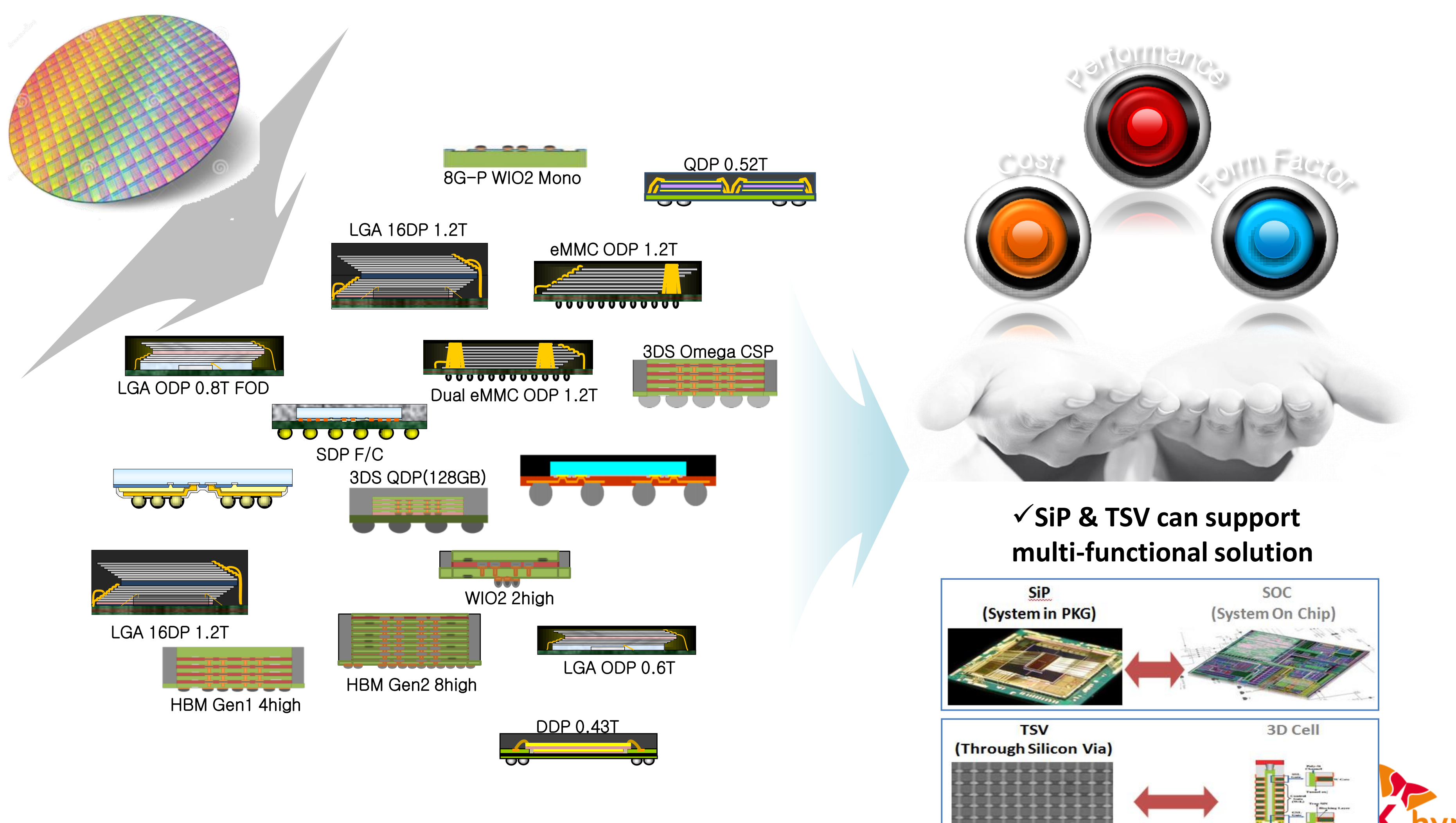
Each application has different memory requirement, but most common are high bandwidth and density based on real time random operation.



SK hynix

Increasing Demand for Packaging Technology

Packaging Technology becomes a key enablement for high performance, small form factor and low cost solution



History of SK Hynix Packaging Technology Development

Reliable memory supplier with advanced packaging technologies

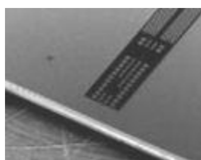
Advanced Technology

2GB DDR2 Wafer level package Memory Module -World Wide 1st (2007.1)

4GB DDR2 Wafer level package Memory Module -World Wide 1st (2008.12)

2Stack Wafer level Package using TSV -World Wide 1st (E/S, 2010.3)

40 nm 2Gb DDR3 8stack using TSV -World Wide 1st (E/S, 2011.3)



WIO1 4KGSD -World Wide 1st (E/S, 2012.11)

Embedded Package 0.235T (E/S, 2013.9)

WLCSP 0.37T (E/S, 2013.9)

128GB DDR4 Module using TSV -World Wide 1st (2014.3)

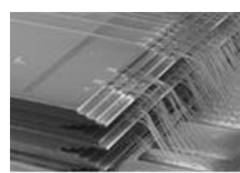
20 nm HBM1 5mKGSD using TSV -World Wide 1st (C/S, 2014.9)

WIO2 Mobile DRAM (4x Faster) using TSV -World Wide 1st (2014.9)

Fan-out 3DS -World Wide 1st (2015.12)

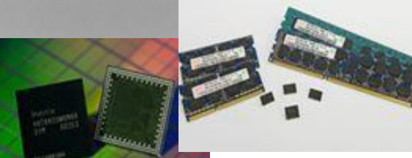
Fan-out WLP (2015.12)

Conventional Technology



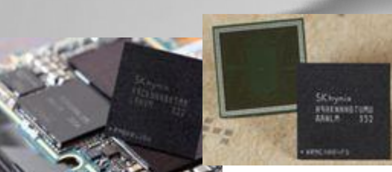
24Stack 1.4T NAND -World Wide 1st (M/S, 2007.9)

8Stack NAND -World Wide 1st (C/S, 2008.12)



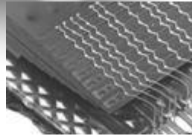
40 nm 2Gb LPDDR2 -World Wide 1st (2010.1)

30 nm 4Gb DDR3 -World Wide 1st (2010.12)



The Highest density 8Gb LPDDR3 -World Wide 1st (2013.6)

20 nm 8Gb LPDDR4 -World Wide 1st (2013.12)



16Stack NAND (E/S, 2014.9)

32Stack NAND (E/S, 2015.12)

2007 | 2008 | 2009 | 2010 | 2011 | 2012 | 2013 | 2014 | 2015

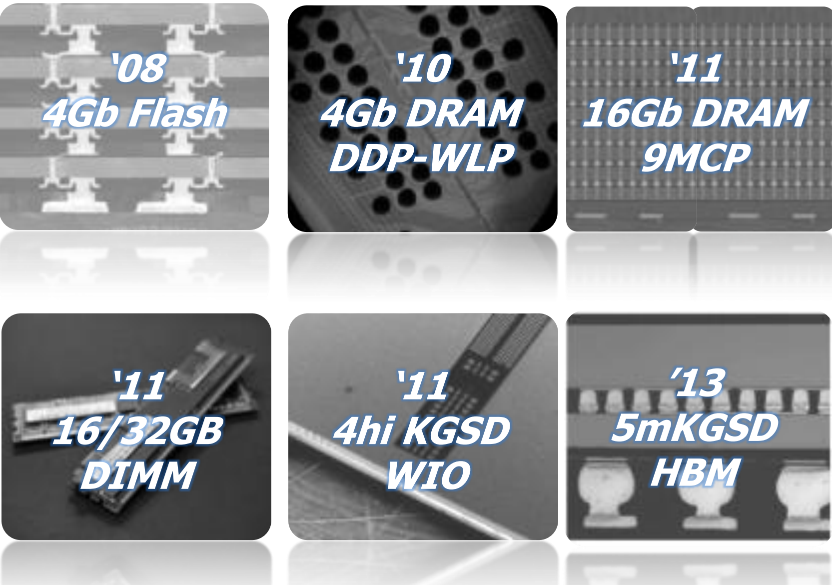
*Developing SK hynix

SK hynix TSV Technology

TSV combines the benefits of LGA and Flip Chip technologies

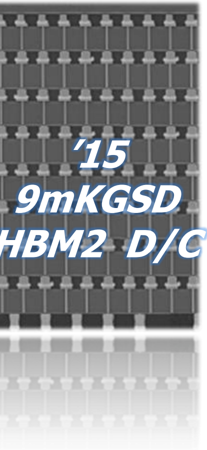
SK hynix TSV development experiences have resulted in mass production of HBM1

SK hynix TSV chronicle



SK hynix's Plan on year 2015

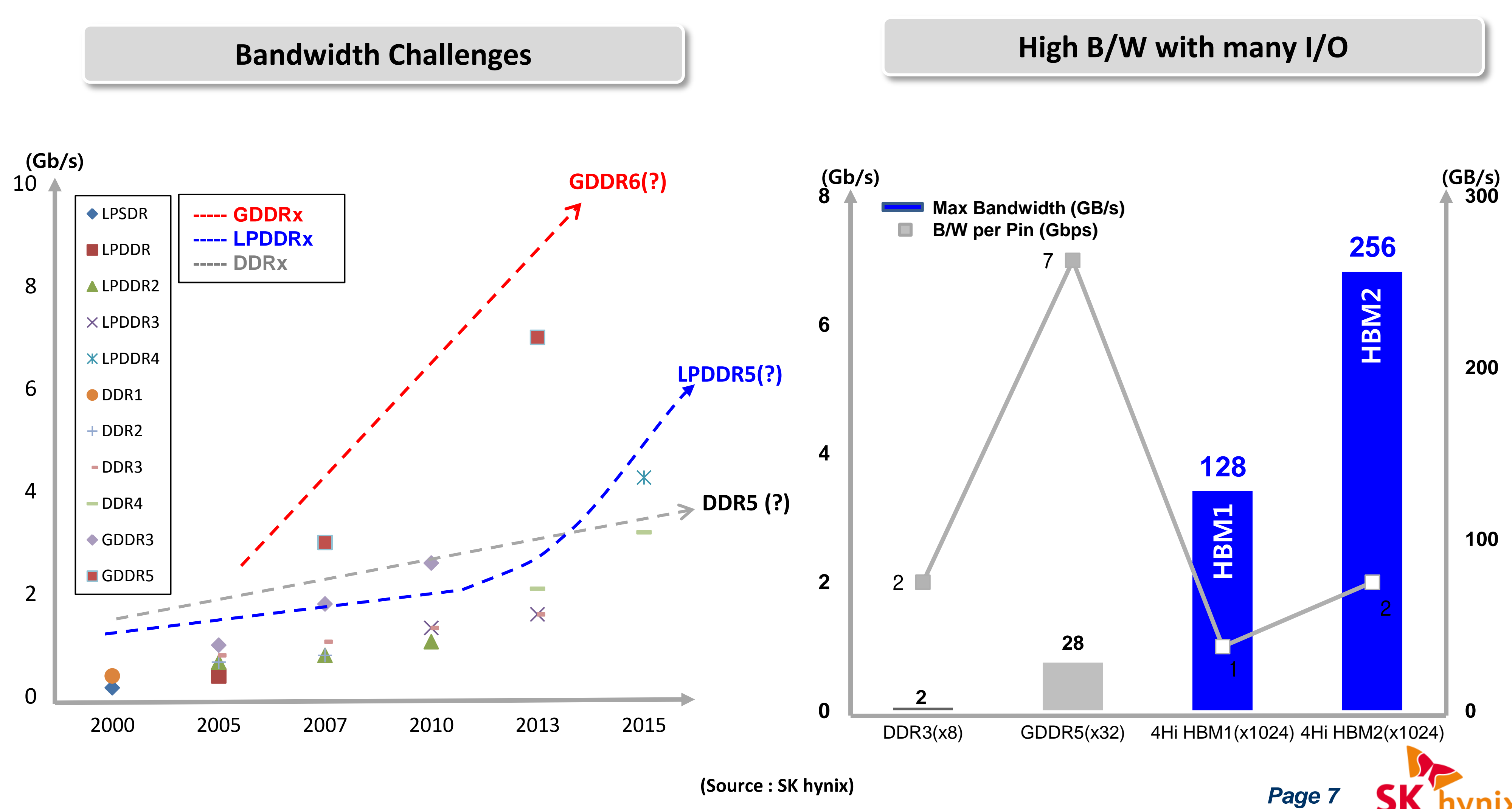
- Volume Production of HBM1
- HBM2 Universal Daisy Chain
- 9mKGSD HBM2 Development



SK hynix

Technology Challenges : Bandwidth

HBM utilizes TSV technology to overcome DRAM bandwidth challenges



(Source : SK hynix)

SK hynix

Technology Challenges : Power Efficiency

Optimized-Speed/pin and Cio of HBM reduces power consumption and increase power efficiency

Power Efficiency

	DDR	DDR2	DDR3	DDR4
Gbps	0.4	0.8	1.6	3.2

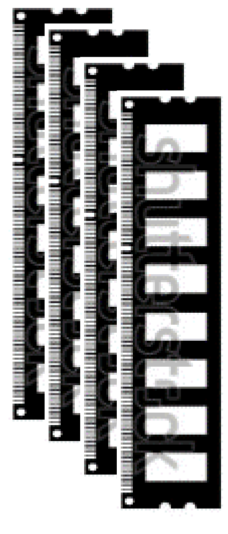
Power Consumption@128GB/s

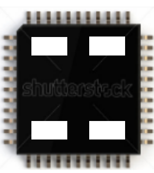
(Source : SK hynix)

Small Form Factor with TSV

1TBps Bandwidth Implementations….

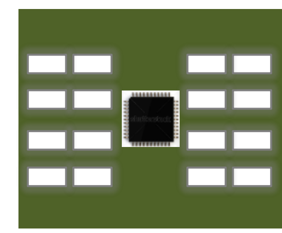
40ea of DDR4-3200 Module is needed

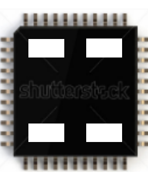




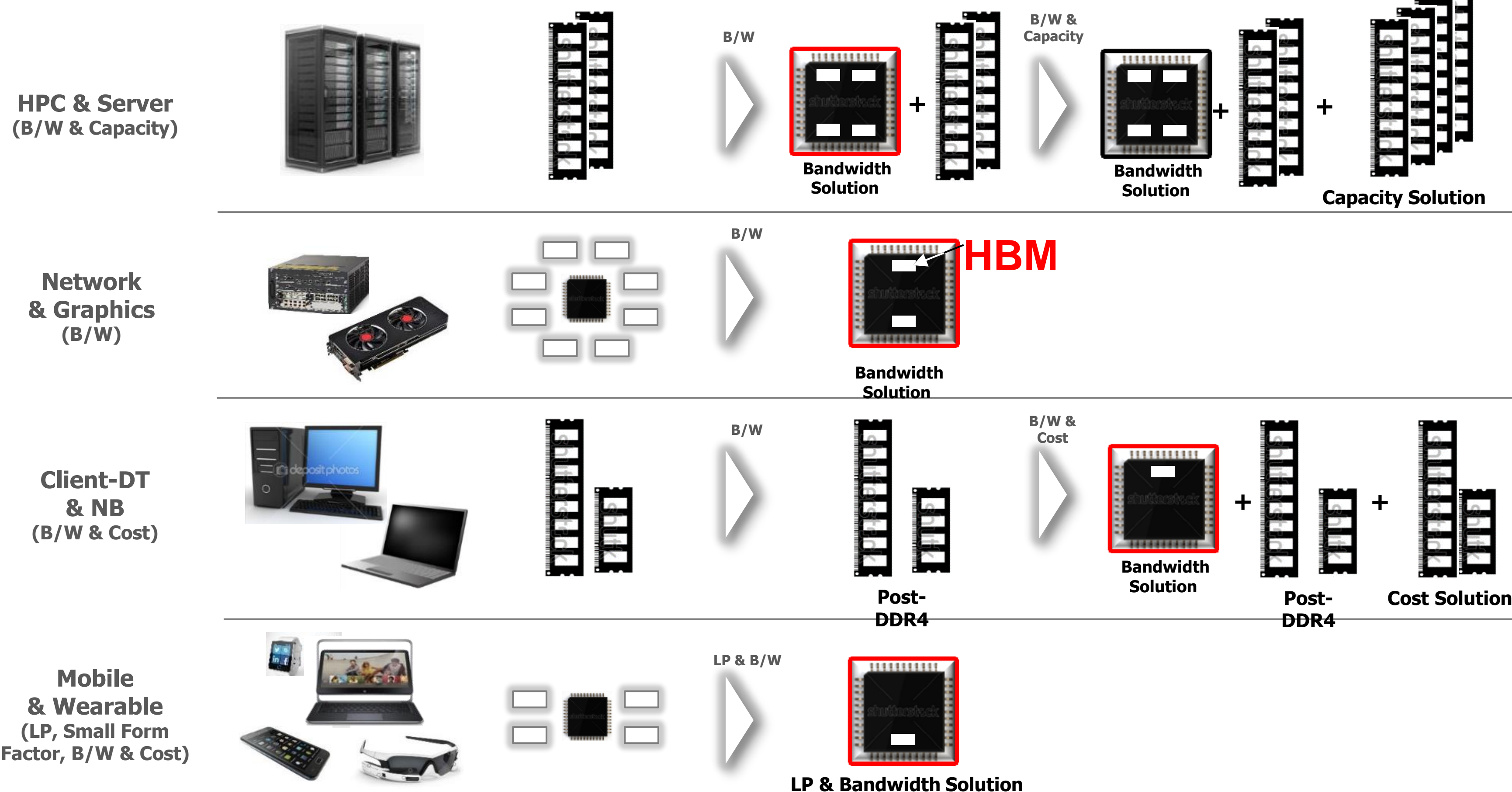
“Only 1ea of 50mmx50mm SiP is needed”

160ea of DDR4-3200 is needed



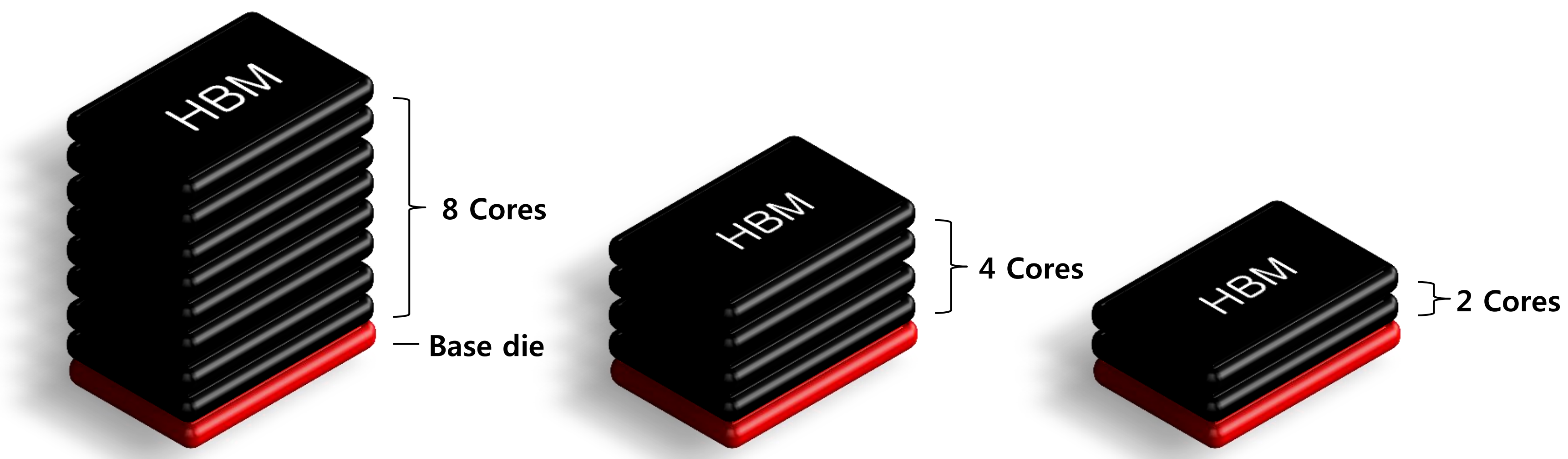


System & Memory Architecture Projection



SK hynix

HBM2 Product Configurations



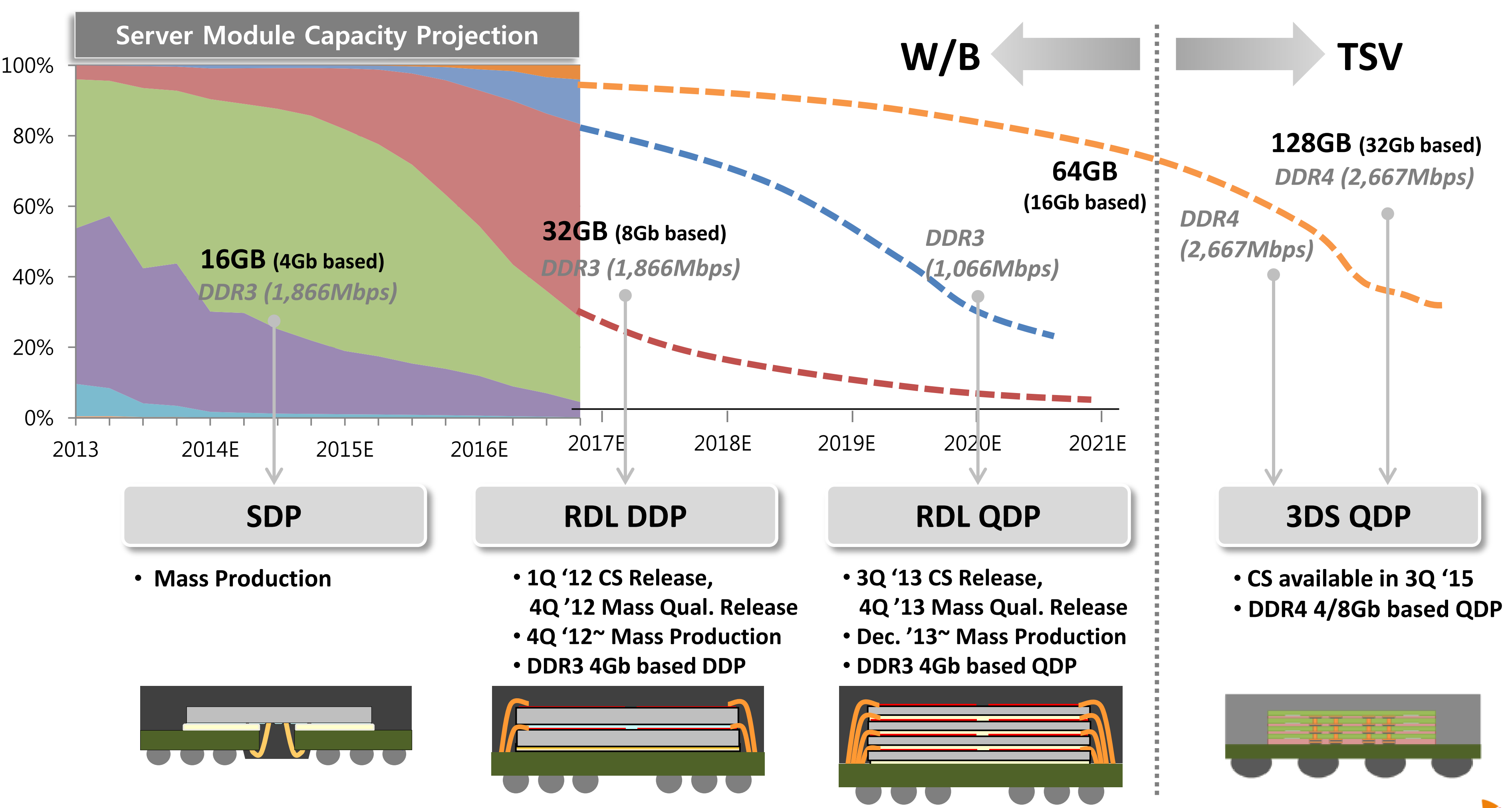
8Gb based	9mKGSD			5mKGSD			3mKGSD		
Density/Cube (GB)	8GB			4GB			2GB		
IO	1024			1024			1024		
Speed/pin (Gbps)	1.0	1.6	2.0	1.0	1.6	2.0	1.0	1.6	2.0
Bandwidth (GB/s)	128	204	256	128	204	256	128	204	256
Usage	HPC, Server			HPC, Server, Graphics, Network			Graphics, Cache		
Config. / system	8 / 6 / 4 Cube			4 / 2 / 1 Cube			2 / 1 Cube		

SK hynix

DDR4 3DS for Server

The highest memory density with high bandwidth requires 3D technology

✓Interconnection paradigm shift; from W/B to TSV



- Mass Production

- 1Q ‘12 CS Release, 4Q ’12 Mass Qual. Release
- 4Q ‘12~ Mass Production
- DDR3 4Gb based DDP

- 3Q ‘13 CS Release, 4Q ’13 Mass Qual. Release
- Dec. ’13~ Mass Production
- DDR3 4Gb based QDP

- CS available in 3Q ‘15
- DDR4 4/8Gb based QDP

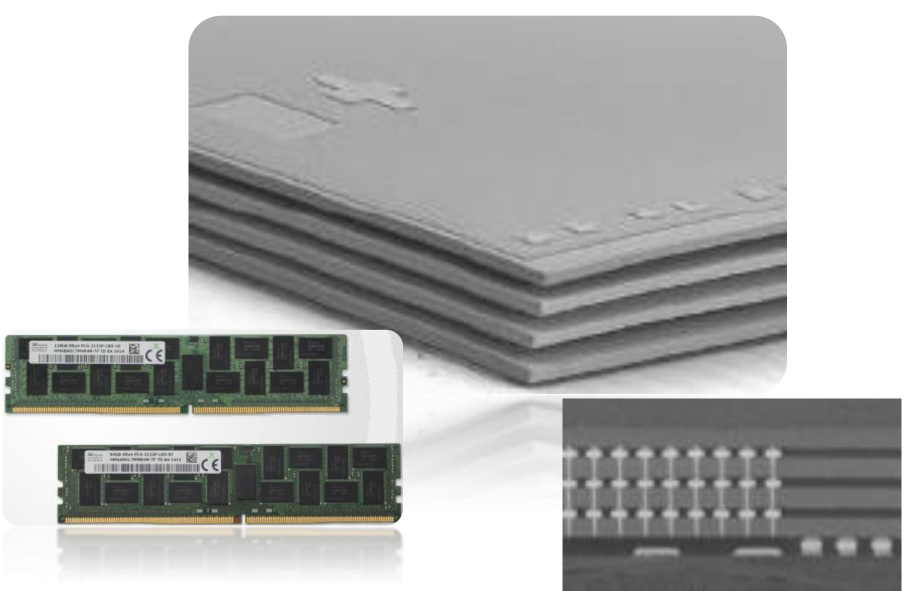
Source: SKH computing marketing
Speed: module based (RDIMM)

SK hynix

3D stacked memory packaging is ready for C/S

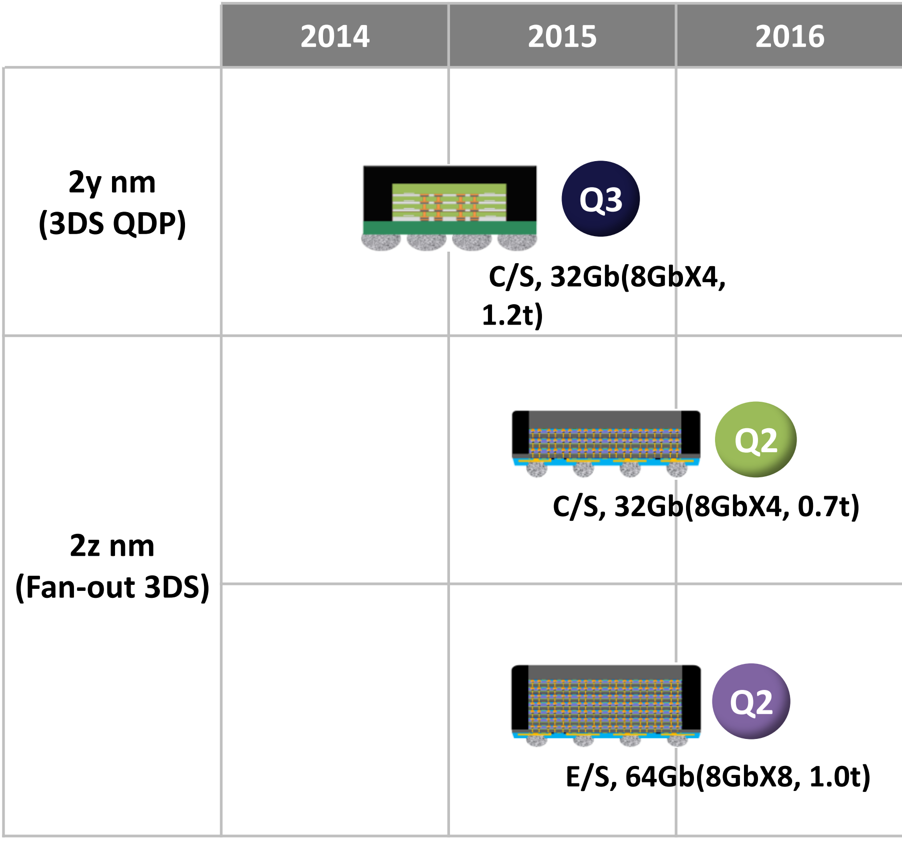
✓ 2y nm 8Gb, SKH's 1st 3DS tech-integrated mass product is available in September '15 as CS

Status



- SK hynix will release 128GB LRDIMM C/S in Apr. 2015.
  - 2znm 8Gb 4-hi stack 3DS is under package level reliability test.

Long Term Roadmap



	2014	2015	2016
2y nm (3DS QDP)		Q3 C/S, 32Gb(8GbX4, 1.2t)	
2z nm (Fan-out 3DS)			Q2 C/S, 32Gb(8GbX4, 0.7t)
			Q2 E/S, 64Gb(8GbX8, 1.0t)

Further work for TSV Technology

- **Advanced TSV Technology**
  - **Fine pitch TSV design aligning with DRAM technology scale**
- **Significant Cost Reduction**
  - **Productivity improvement, Advanced equipment, Test Time Reduction, etc.**
- **Improvement of stacking technology**

SK hynix